Bipolar Junction Transistor (BJT)

It is three terminal devices Emitter, Base and Collector constricted from two P-N junctions. The Base is usually made thin and has a load doping level to minimize the number of carrier lost by recompilation in base region on the emitter and collector having a high doping level with the emitter is higher than collector, it is a two diode back to back connected the symbols for both type shown in fig (1-1)

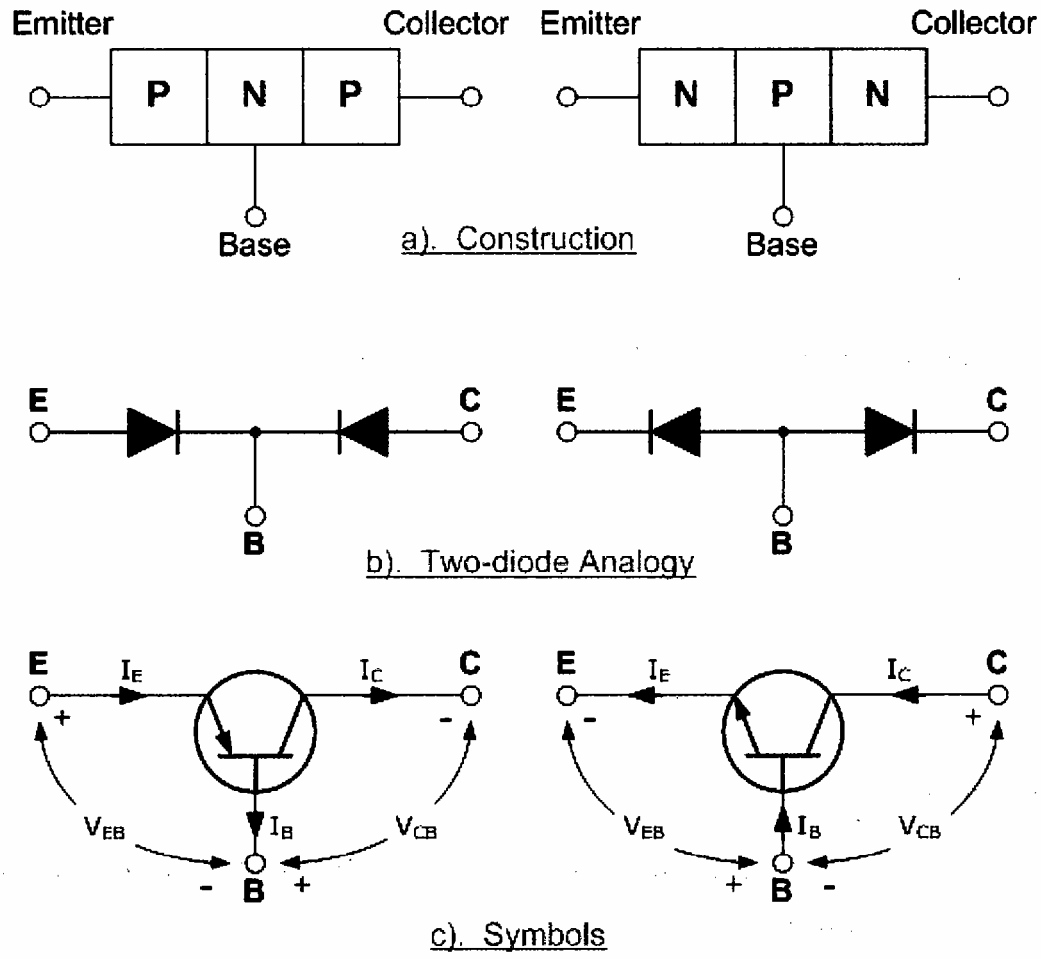


Fig (1-1)

There are basically three possible ways to connect a **Bipolar Transistor** within an electronic circuit with each method of connection responding differently to its input signal as the static characteristics of the transistor veray with each circuit arrangement.

1- Common Base Configration ***: has Voltage Gain but no Current Gain.***

2- Common Emitter Configration : ***has both Voltage and Current Gain.***

3- Common Collector Configration : ***has Current Gain but no Voltage Gain.***

Transistor operation region

1. Saturation region

B-E and B-C junctions are forward it works as close switch.

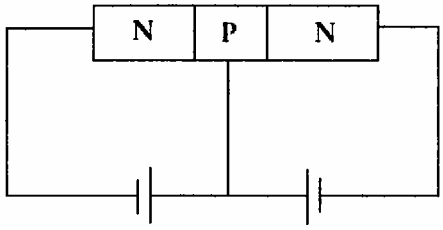


Fig (1-2)

2. Cutoff region

Both junctions are reversed it behave as an open switch.

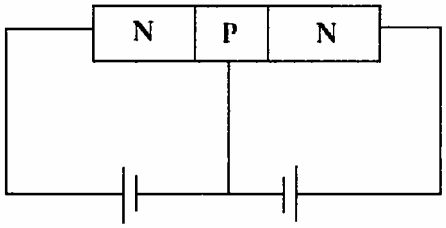


Fig (1-3)

3. Active region

Base -Emitter junction is forward and Base-collector is reverse. Transistor works as an amplifier

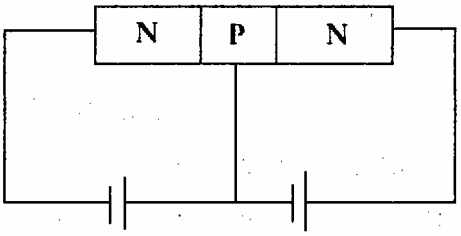


Fig (1-4)

DC Biasing—BJTs

The analysis or design of a transistor amplifier requires a knowledge of both the dc and ac response of the system. The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In this Section we specify the range for the BJT amplifier

$$V_{BE} = 0.7\ \text{V}$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

$$\alpha_{dc} = \frac{I_C}{I_E}$$

1. FIXED-BIAS CIRCUIT

*Forward Bias of Base-Emitter

Consider first the base–emitter circuit loop of Fig. (1-6). Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

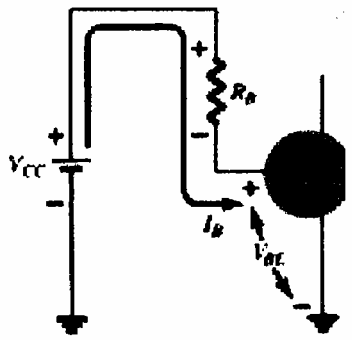


Fig (1-6)

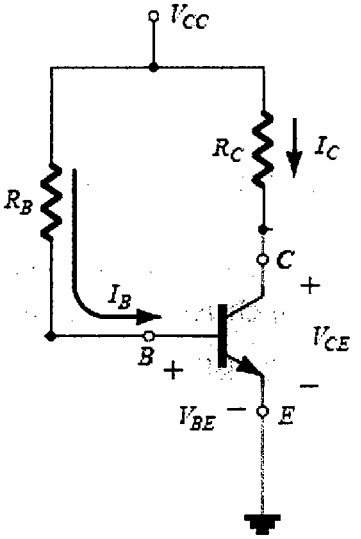


Fig (1-5)

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 1-7 with the indicated direction of current I_C and the resulting polarity acrossR_c. The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B$$

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 1-7 will result in the following:

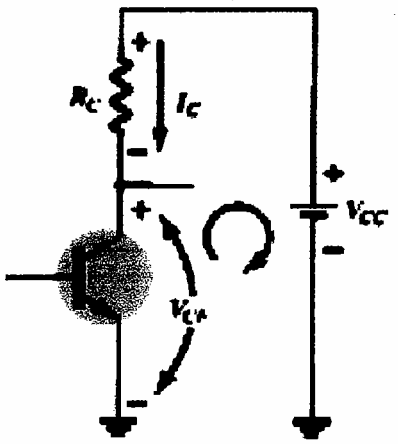


Fig (1-7)

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

Transistor Saturation

$I_c.sat$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \quad \text{at } V_{CE} = 0$$

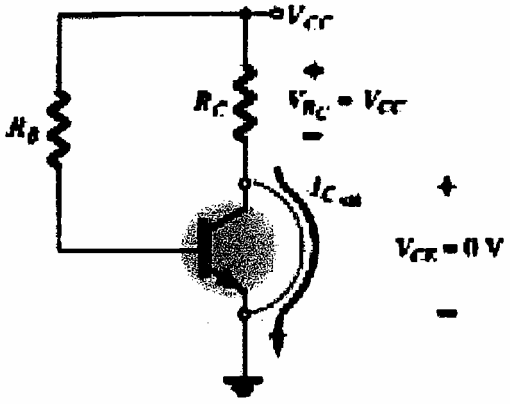


Fig (1-8)

Load-Line Analysis

The network of Fig. 1.8 establishes an output equation that relates the variables I_c and V_{CE} in the following manner

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - (0)R_C$$

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}}$$

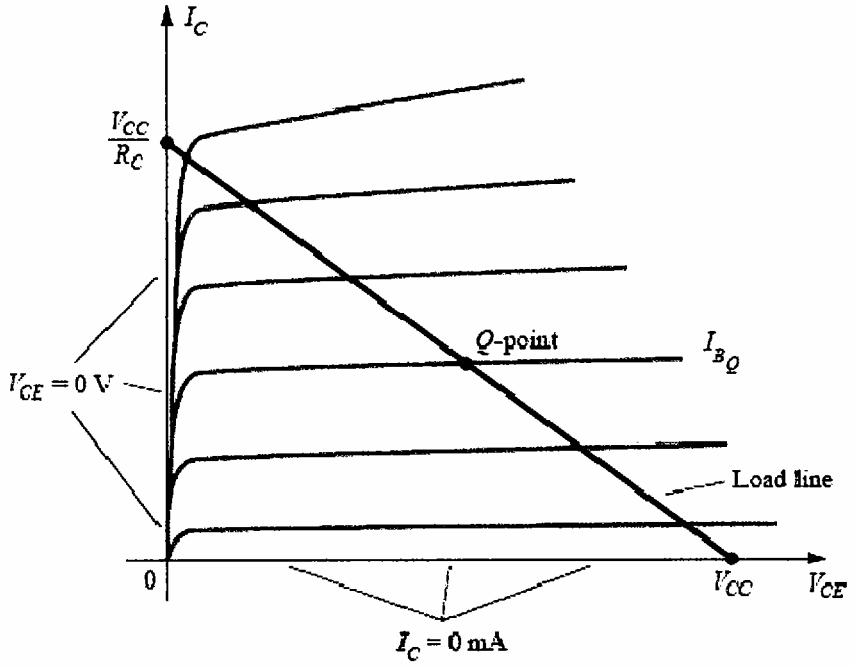


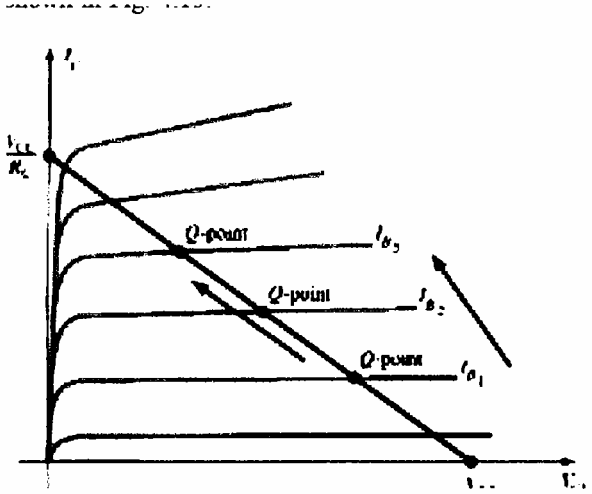
Fig (1-9) c/cs of transistor

Fig(1-9) show Fixed-bias load line.

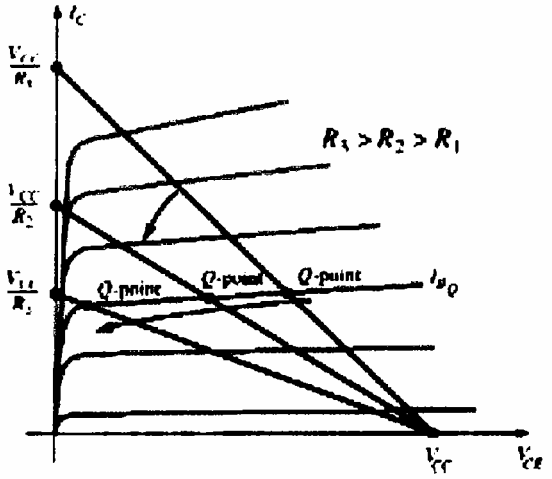
If the level ofI_B is changed by varying the value of R_B the *Q*-point moves up or down the load line as shown in Fig. 1-10.

If V_{cc} is held fixed and R_c changed, the load line will shift as shown in Fig. 1-11.

If *IB* is held fixed, the *Q*-point will move as shown in the same figure. If *RC* is fixed and *VCC* varied, the load line shifts as shown in Fig. 1-12.



Fig(1-10) Movement of Q-point with increasing levels of I_B line and Q-point



Fig(1-11)Effect of increasing levels of R_C on the load

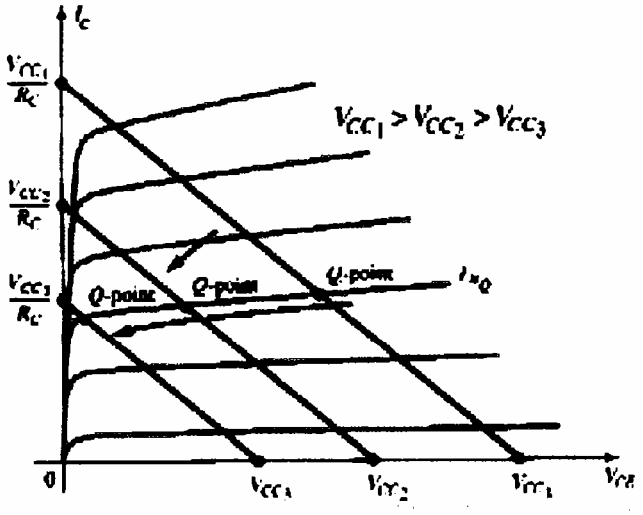


Figure 1-12 Effect of lower values of V_{CC} on the load line and Q-point

Example :1

Given the load line of Fig. 1-13 and the defined Q-point, determine the required values ofV_{CC}, R_C, and R_B for a fixed-bias configuration.

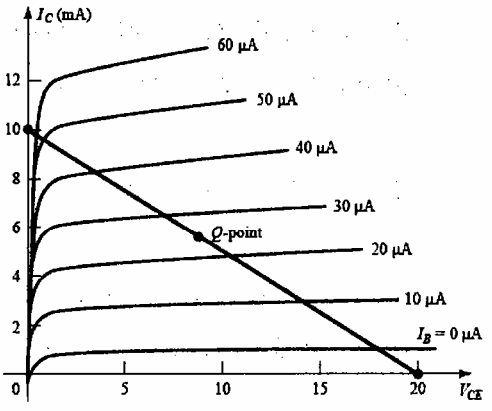


Fig (1-13)

$$V_{CE} = V_{CC} = 20\ \text{V at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\text{ V}}{10\text{ mA}} = 2\text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{ V} - 0.7\text{ V}}{25\ \mu\text{A}} = 772\text{ k}\Omega$$

2. EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig. 1-14 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

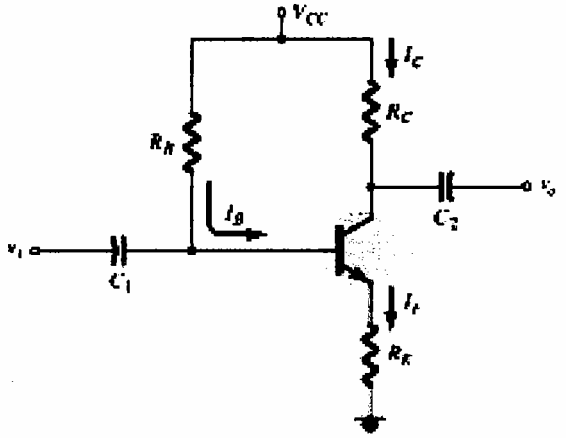


Figure (1-14) BJT bias circuit with emitter resistor.

*Base–Emitter Loop

The base–emitter loop of the network of Fig. 1-14 can be redrawn as shown in Fig. 1-15. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1)I_B$$

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

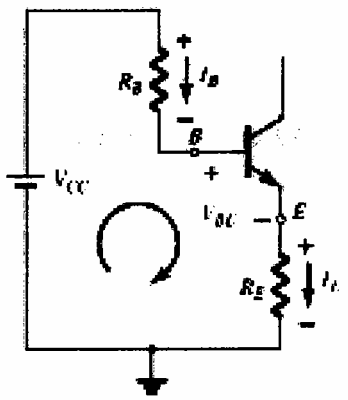


Fig (1-15) Base–emitter loop.

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}}$$

*Collector–Emitter Loop

The collector–emitter loop is redrawn in Fig. 1-16. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

The single-subscript voltage *VE* is the voltage from emitter to ground and is determined by

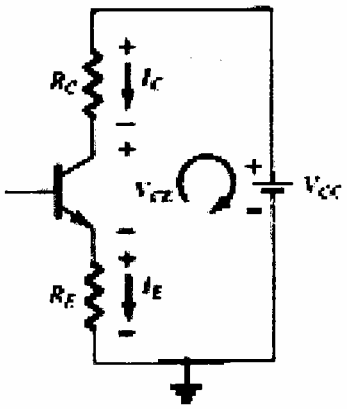


Fig (1-16) Collector-Emitter loop

$$\boxed{V_E = I_E R_E}$$

$$V_{CE} = V_C - V_E$$

$$\boxed{V_C = V_{CE} + V_E}$$

$$\boxed{V_C = V_{CC} - I_C R_C}$$

The voltage at the base with respect to ground can be determined from

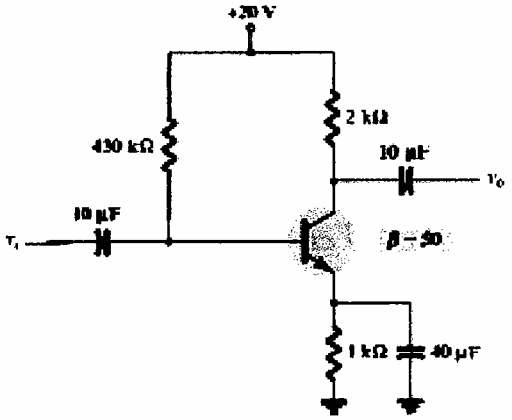
$$\boxed{V_B = V_{CC} - I_B R_B}$$

Or

$$\boxed{V_B = V_{BE} + V_E}$$

Example:2

For the emitter bias network of Fig. 1-17, determine:
(a) I_B, (b) I_C, (c) V_{CE}, (d) V_C, (e) V_E, (f) V_B, (g) V_{BC}.



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\ mA}$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
(c) $= \mathbf{13.97\ V}$

Fig. 1-17

(d) $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\ V}$

(e) $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\ V}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\ V}$

(f) $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\ V}$

(g) $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\ V}$ (reverse-biased as required)

Example:3

Determine the following for the fixed-bias configuration of Fig. 1-18
(a) I_{BQ} and I_{CQ} (b) V_{CEQ} (c) V_B and V_C (d) V_{BC}

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V}$$
$$V_C = V_{CE} = \mathbf{6.83\ V}$$

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

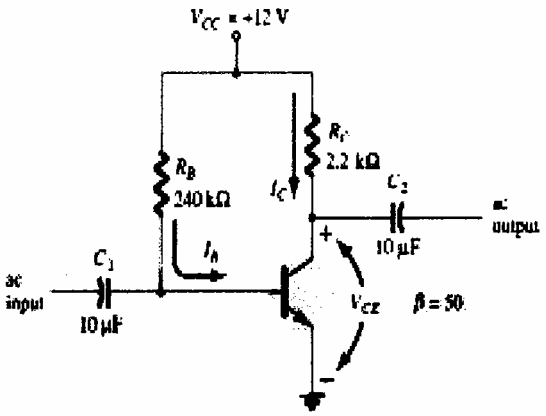


Fig (1-18) dc fixed-bias circuit

Example:4

Prepare a table and compare the bias voltage and currents of the circuits of Figs1-17 and Fig. 1-18 for the given value of β= 50 and for a new value of β= 100. Compare

the changes in I_C and V_{CE} for the same increase in β

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of .β I_B is the same and V_{CE} decreased by 76%. Using the results calculated in Example 2 and then repeating for a value of β = 100, we have the following

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C or at least reducing the overall change in I_C due to the change in β. The change in

V_{CE} has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 1-17 for the same change in β

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

Load-Line Analysis

The collector–emitter loop equation that defines the load line is the following

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing I_C= 0 mA gives

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}}$$

as obtained for the fixed-bias configuration. Choosing V_{CE}= 0 V gives

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\text{ V}}$$

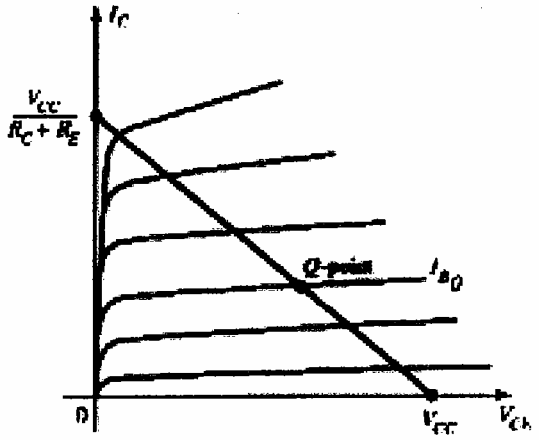


Fig (1-19) Load line for the emitter-bias configuration

3. *VOLTAGE-DIVIDER BIAS*

In the previous bias configurations the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta